UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/620,498	07/20/2000	YOSHIO HAGIHARA	15162/02240	3562

24367 7590 08/24/2005

SIDLEY AUSTIN BROWN & WOOD LLP
717 NORTH HARWOOD
SUITE 3400
DALLAS, TX 75201

EXAMINER	
AGGARWAL, YOGESH K	
ART UNIT	**PAPER NUMBER**
2615	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/620,498	HAGIHARA, YOSHIO	
	Examiner	Art Unit	
	Yogesh K. Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6-8,10-18,20 and 23-39* is/are pending in the application.

4a) Of the above claim(s) *4,5,9,19,21 and 22* is/are withdrawn from consideration.

5)☒ Claim(s) *10-13,15,17,18,20,23,24 and 30-39* is/are allowed.

6)☒ Claim(s) *1,2,6-8,11,14,16 and 25-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claims 1 and 25 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 6, 11, 16 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dierickx (US PG-PUB # 2001/0045508), Nakamura et al. (5,289,286) and in further view of Takahashi (US Patent # 6188109).

[Claims 1,25]

Dierickx teaches an image-sensing apparatus (figure 1) comprising a plurality of pixels the pixels (10) each comprising comprise a photoelectric conversion portion (1) and a FET (7) that has a photosensitive element for producing an electric signal in accordance with amount of incident light and that outputs a signal obtained by converting the electric signal natural-logarithmically (Paragraphs 25 and 26, figures 1 and 2). Dierickx further teach that to calibrate the PRNU (pixel response non uniformities or variation in sensitivity of the photoelectric conversion portion) of each pixel, a reading of the pixel is done with a predetermined current and added with a current

injected from the current source 2 (injecting an electric charge into the photoelectric conversion portion, Paragraph 27). A controller would be inherently taught. Dierickx does not explicitly teach an integrator circuit.

However Nakamura et al. teaches an integrator circuit (figure 13, transistor 2b and capacitor 3) that integrates the signal output from the photoelectric conversion portion (figures 12 and 13, photoelectric portion 1) so that a signal integrated by the integrator circuit is fed by way of the lead-out path (V_o) to the output signal line (col. 30 lines 30-60).

Therefore taking the combined teachings of Dierickx and Nakamura, it would have been obvious to one skilled in the art at the time the invention was made to have been motivated to have an integrator circuit that integrates the signal output from the photoelectric conversion portion so that a signal integrated by the integrator circuit is fed by way of a lead-out path to the output signal line as taught by Nakamura into the circuit of Dierickx in order to integrate and store the charges accumulated on the photoelectric portion to obtain a strong signal that facilitates the signal processing.

Dierickx in view of Nakamura fails to explicitly teach that variations in sensitivity region that can be detected by causing an electric charge that is indicative of the threshold voltage of the FET. However Takahashi discloses a device 102 wherein the gate voltage is determined by the Equation 1 and a sensitivity to detect abnormalities is determined by a combination of three variables, that is, a capacitance C (sense), a capacitance C (MOSFET) and a gate threshold voltage of the transistor M1 in order to have a high detection sensitivity can be obtained by freely selecting these three variables (col. 23 lines 46-54). Therefore in order to measure

sensitivity an electric charge that is indicative of threshold voltage would have to be inherently injected.

Therefore taking the combined teachings of Dierickx, Nakamura and Takahashi, it would have been obvious to one skilled in the art at the time the invention was made to have been motivated to have variations in sensitivity region can be detected by causing an electric charge that is indicative of the threshold voltage of the FET in order to have a high detection sensitivity can be obtained by freely selecting these three variables as taught in Takahashi (col. 23 lines 46-54).

[Claim 2]

Dierickx discloses an array of pixels are arranged a matrix (Paragraphs 3 and 4).

[Claims 6 and 27]

Dierickx discloses an amplifying transistor (48) in third embodiment (figure 4) (Paragraph 34) in order to amplify the signal readout within the pixel. The leadout path is taught in Nakamura (col. 30 lines 30-60).

[Claims 11 and 26]

Dierickx discloses a first transistor (7) for reading out the signal acquired in the photosensitive element and converted to a voltage drop across the first transistor (Paragraph32). A transistor is read as a switch that is used for selecting pixels one after another and turning on and off the electric signal output line.

[Claim 16]

Dierickx teaches to calibrate the PRNU (pixel response non uniformities or variation in sensitivity of the photoelectric conversion portion) of each pixel, a reading of the pixel is done

with a predetermined current and added with a current injected from the current source 2 (injecting an electric charge into the photoelectric conversion portion, Paragraph 27). A controller would be inherently taught. Dierickx further teaches that the method is advantageous because no illumination of light is necessary which means that the controller detects variations in sensitivity of the photoelectric conversion portion of the individual pixels with the photosensitive elements of the individual pixels kept in a dark state.

4. Claims 7, 8 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dierickx (US PG-PUB # 2001/0045508), Nakamura et al. (5,289,286), Takahashi (US Patent # 6188109) and in further view of Kuroda (6,512,543).

[Claims 7 and 28]

Dierickx, Nakamura in view of Takahashi teach the limitations of claim 6 and 25 but fails to teach load resistors or constant current sources connected to the output serial line, a total number of the load resistors or constant current sources being smaller than a total number of pixels.

Nevertheless, Kuroda teaches a CMOS image sensor wherein constant current sources (Figure 1, Element 44) are connected to the output signal line (Figure 1, Element 43), a total number of constant sources being smaller than the total number of pixels (There are 3 constant current sources for 9 pixels). The combination of the constant current sources would have been obvious, both the inventions of Moose and Kuroda are of CMOS image sensors. The load transistor in Kuroda serves as a constant current source for the source follower circuit including the load transistor and it determines an electric current flowing in that source follower circuit column 7, Line 60 through Column 8, line 9).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to configure the invention of CMOS image sensor of Dierickx, Nakamura and in view of Takahashi with the constant current source of Kuroda in order to determine the current flowing through the source follower circuit.

[Claim 8]

Kuroda further discloses wherein the constant-current sources each comprise a resistive transistor (44) having a first electrode connected to the output signal line, a second electrode connected to a direct- current voltage, and a control electrode connected to a direct-current voltage (44).

5. Claims 14 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dierickx (US PG-PUB # 2001/0045508), Nakamura et al. (5,289,286), Takahashi (US Patent # 6188109) and in further view of Hynecek (US 6,323,479).

[Claims 14 and 29]

Dierickx, Nakamura in view of Takahashi teach the limitations of claims 1 and 25 but fails to teach wherein, during image sensing, the pixels can operate selectively either in a first state in which the photoelectric conversion portion converts the electric signal linearly and in a second state in which the photoelectric conversion portion converts the electric signal natural logarithmically.

However, Hynecek teaches a sensor pixel linear and logarithmic response, further disclosing, during image sensing, the pixels can operate selectively either in a first state in which the photoelectric conversion portion converts the electric signal linearly and in a second state in which the photoelectric conversion portion converts the electric signal natural logarithmically

(Abstract, Column 2, Line 60 through Column 3, Line 31). The logarithmic range begins after the region of sub-threshold conduction begins. The device of Hynecek provides for two regions of predetermined voltage. When the first predetermined is exceeded, the logarithmic response begins. When the second predetermined voltage is reached, the linear response begins.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to configure solid state imaging device of Dierickx, Nakamura in view of Takahashi with the sensor pixel with linear and logarithmic response of Hynecek in order to obtain white balance without the use of multiplication and division which are needed to be performed every time the color temperature changes during the linear region. Therefore in order to simplify the circuit the white balance are performed for logarithmic response without the use of multiplication and division.

Allowable Subject Matter

6. Claims 10, 12, 13, 15, 17, 18, 20-24, 30-34, 35-39 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter: Regarding claims 30-34, 35-39 the prior art fails to suggest or teach An image-sensing apparatus comprising a plurality of pixels, the pixels each comprising a photoelectric conversion portion including "…. a first transistor having a first electrode connected to the second electrode of the photosensitive element, a second electrode, and a control electrode, the first transistor receiving an output current from the photoelectric element, the first transistor having a plurality of potentials applied to the second electrode among other elements".

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
August 22, 2005

DAVID L. OMETZ
SUPERVISORY PATENT
EXAMINER